What is claimed is:

1. A poly-crystalline thin film transistor, comprising:

a buffer layer on a substrate;

a poly-crystalline semiconductor layer on the buffer layer, the poly-crystalline layer including a channel layer, offset regions along sides of the channel layer, sequential doping regions along sides of the offset regions, and drain and source regions along sides of the sequential doping regions, wherein the doping concentration of the sequential doping regions are greater near the drain and source regions than near the offset regions;

a gate insulation layer on the semiconductor layer;

a gate electrode on the gate insulation layer, wherein the gate electrode is comprised of a main gate electrode and of auxiliary gate electrodes;

an interlayer over the gate electrode; and

source and drain electrodes on the interlayer, wherein the source electrode contacts the source region through a source contact hole in the interlayer, and wherein the drain electrode contacts the drain region through a drain contact hole in the interlayer.

2. The thin film transistor of claim 1, wherein the gate insulation layer has a first thickness over the channel layer and over the source and drain regions, a second thickness over the offset regions, and a tapered thickness over the sequential doping regions.

3. The thin film transistor of claim 2, wherein the main gate electrode is formed over the channel layer.

4. The thin film transistor of claim 2, wherein the auxiliary gate electrodes extend over the offset regions.

5. The thin film transistor of claim 2, wherein the sequential doping regions have a higher doping concentration near the source and drain regions than near the offset regions.

6. The thin film transistor of claim 1, wherein the offset regions are undoped.

7. The thin film transistor of claim 1, wherein the channel layer is undoped.

8. The thin film transistor of claim 1, further comprising:

a passivation layer over the interlayer and over the source and drain electrodes; and

a pixel electrode on the passivation layer, wherein the pixel electrode layer contacts the drain electrode through a hole in the passivation layer.

9. The thin film transistor of claim 1, wherein the substrate is glass.

10. A poly-crystalline thin film transistor fabricating method comprising:

forming a poly-crystalline semiconductor layer on a buffer layer on a substrate;

forming a gate insulation layer over the poly-crystalline semiconductor, wherein the gate insulation layer is formed with a first thickness at a channel position and at source and drain positions, wherein the gate insulation layer is formed with a second thickness at

offset positions, and wherein the thickness of the gate insulation layer tapers in sequential doping positions from the second thickness to the first thickness;

forming a gate structure on the gate insulation layer, wherein the gate structure includes a main gate electrode over the channel position and auxiliary gate electrodes over the offset positions;

impurity doping the semiconductor layer through exposed portions of the gate insulation layer while using the gate structure as a mask to define sequential doping regions that are aligned with the sequential doping positions, and source and drain regions that are aligned with the source and drain positions.

11. The method of claim 10, further including forming an interlayer over the gate insulation layer and over the gate electrode; and

forming contact holes through the interlayer to expose the source and drain electrodes.

12. The method of claim 11, further including forming drain and source electrodes that contact the source and drain regions through the contact holes.

13. The method of claim 10, wherein forming a poly-crystalline semiconductor layer includes depositing a poly-crystalline silicon on the buffer layer.

14. The method of claim 10, wherein forming a poly-crystalline semiconductor layer includes depositing the buffer layer on a glass substrate.

15. The method of claim 10, wherein forming a poly-crystalline semiconductor layer comprises:

depositing an amorphous silicon on the buffer layer; and

laser-annealing the amorphous silicon.

16. The method of claim 10, wherein forming the gate insulation layer comprises:

forming a first insulation layer on the poly-crystalline semiconductor layer;

forming a second insulation layer on the first insulation layer; and

etching the second insulation layer.

17. The method of claim 10, wherein impurity doping the semiconductor layer includes forming an impurity concentration in the sequential doping region that depends on the taper of the gate insulation layer in the sequential doping positions.

18. The method of claim 12, further comprising forming a passivation layer over the source and drain electrodes and over the interlayer.

19. The method of claim 18, further comprising forming a drain contact hole through the passivation layer, wherein the drain contact hole exposes the drain electrode.

20. The method of claim 19, further comprising forming a drain contact electrode on the passivation layer, wherein the drain contact electrode contacts the drain electrode through the drain contact hole.